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Analysis of interfacial thermal stresses of chip-substrate structure

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Abstract

The interfacial thermal stresses of the chip-substrate structure near free edges play an important role in determining the reliability of electronic packaging structures. According to the heat conduction mechanism of integrated circuits, the temperature field of the chip and the substrate is derived when the chip works in a steady state. A simple method is developed to determine the stress field of the chip and the substrate, which can exactly satisfy the traction-free boundary conditions and continuity conditions on the interface. The corresponding stress field is solved in terms of the variational principle. Finally, the effect of geometrical parameters of the chip and the substrate on stress concentration is analyzed in detail. © 2001 Elsevier Science Ltd. All rights reserved.

Keywords: Electronic packaging; Chip-substrate structure; Interfacial thermal stresses; Stress concentration

1. Introduction

The chip-substrate structure is an important part of integrated circuit (IC) devices in which the chip produces heat and the substrate, besides the function that protects the IC from its environment and provides the mechanical support for the chip, has the important function of dissipating heat from the chip. Due to variations in the power input and the ambient temperatures, IC devices undergo several power and thermal cycles during operation. Thus, the chip and the substrate are susceptible to severe and local stresses along the interface between the chip and the substrate, especially near free edges. These interfacial stresses which are induced by the thermal mismatch expansion between the chip and the substrate may cause the thermal fatigue crack propagation and delamination of the chip-substrate structure and make IC devices invalid. Therefore, the analysis of thermal stresses along the interface between the chip and the substrate is very important for guiding the design of packaging structures.

For assemblies used in electronic devices, Chen and Nelson (1979) investigated the stress distribution in bonded materials due to their thermal expansion mismatch. Suhir (1986) calculated peeling and shear

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stresses at free edges by using an interfacial compliance coefficient and showed the higher stress concentration. Based on his previous work (Suhir, 1986), Suhir (1989) presented an approximate method and estimated stresses in layers and interfacial stresses between layers. Kuo (1989) and Lee and Jasiuk (1991) investigated the asymptotic behavior of stresses near the tips of bonded interfaces in layer structures. Based on the variational principle, Yin (1991) developed a numerical method to address this issue. At present, this method has been developed to study the layer beams and laminates subjected to mechanical and thermal loads. Suhir (1995) analyzed the interaction of the global and the local thermal mismatch stresses in an elongated bi-material rectangular plate. To overcome the nonequilibrium of peeling stress distribution, Jiang et al. (1997) presented an improved method on the beam, which is simple and accurate to engineering application.

For the analysis of bi-material structures subjected to thermal loads, the finite element method (FEM) is a powerful tool. Many researchers applied this method to analyze the interfacial stresses induced by thermal loads (e.g., Suganuma et al., 1984; Blanchard and Watson, 1986; Gerstle and Chambers, 1987 etc.). However, Lau (1989) pointed out that the interfacial stresses near free edges, predicted by the conventional displacement-based FEM, are unreliable. He suggested a modified FEM, based on the displacement approach with nodal strain calculation, to obtain more accurate solutions near free edges. Pionke and Wempner (1991) compared elementary approximations with refined results via FEM and pointed out that the deflection is given with reasonable accuracy by simple approximations, but the severe interfacial stresses are revealed only by FEM.

For the analysis of interfacial thermal stresses in the chip-substrate structure, all the works mentioned above assume that the distribution of temperature fields in the chip and the substrate is uniform or linear. Obviously, this does not conform to the factual distribution of temperature fields. For this purpose, the heat conduction mechanism of the system should be considered in analyzing interfacial thermal stresses of the chip-substrate structure. In the present paper, the temperature field of the system in a steady state is solved by taking into account the heat conduction mechanism of ICs. According to Yin (1995), a simple method is used to determine the stress field of the chip and the substrate, which satisfy all the traction-free boundary conditions and continuity conditions along the interface. Therefore, this method is more reasonable than other approximations. Finally, the effect of geometrical parameters of the chip and the substrate on interfacial thermal stresses near free edges is studied by the approach mentioned above and numerical results are obtained.

In what follows, a two-dimensional Cartesian coordinate system is adopted where the position of a point is denoted by the coordinate (x, y) . In addition, the summation convention over repeated Latin indices is adopted over the range 1–2. Furthermore, a comma denotes partial differentiation, for example, $f_{,1}$ and $f_{,2}$ mean $\partial f / \partial x$ and $\partial f / \partial y$, respectively.

2. Temperature field of chip-substrate structure

2.1. Statement of the problem

As shown in Fig. 1, consider a chip-substrate structure where the chip is considered as a heat source and the heat from the chip is dissipated through the substrate. Since the adhesive layer between the chip and the substrate is very thin, its thermal resistance can be omitted and only the thermal resistance of the chip and the substrate is considered. The thermal conductivity, width and thickness of the chip are denoted by the symbols k_1 , $2a$ and t_1 , respectively, while the corresponding parameters of the substrate are represented by k_2 , $2b$ and t_2 . Since the size along the direction perpendicular to the xy -plane is larger, the present problem can be considered as the plane-strain problem. To solve the present problem, we introduce the symbol q to

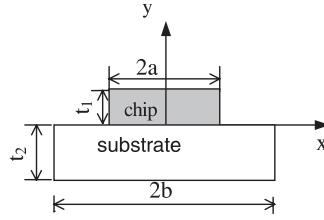


Fig. 1. Chip-substrate structure.

denote the heat flux due to the chip on the upper surface of the substrate, considered as uniformly distributed over the chip.

2.2. Basic equations of temperature field

Consider the case in which the chip is a larger and thinner plate. It can be assumed that the heat from the chip is dissipated only along the thickness direction, as shown in Fig. 2(a). When the chip works in a steady state, the temperature field in the chip will not vary with time and can be denoted by $T_1(x, y)$. The model of heat conduction in the substrate is showed in Fig. 2(b). Here, the uniform heat flux with the density q is applied to the top surface of the substrate, which is contacted by the chip. The bottom surface of the substrate is convectively cooled and other surfaces are adiabatic.

When the temperature field of the substrate is denoted by $T_2(x, y)$, the basic equations in the chip and the substrate can be written as

Governing equations

$$q = k_1 \frac{\partial T_1}{\partial y}, \quad (1)$$

$$\nabla^2 T_2 = 0. \quad (2)$$

Boundary conditions

$$\left. \frac{\partial T_2}{\partial y} \right|_{y=0} = \frac{q}{k_2}, \quad |x| \leq a, \quad (3a)$$

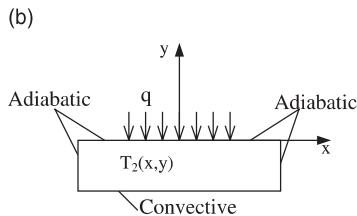
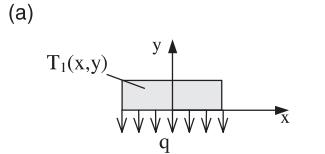


Fig. 2. Heat conduction model of chip and substrate.

$$\frac{\partial T_2}{\partial y} \Big|_{y=0} = 0, \quad a \leq |x| \leq b, \quad (3b)$$

$$\frac{\partial T_2}{\partial y} \Big|_{y=-t_2} = \frac{h}{k_2} (T_2(x, -t_2) - T_f), \quad |x| \leq b, \quad (3c)$$

$$\frac{\partial T_2}{\partial x} \Big|_{|x|=b} = 0, \quad -t_2 \leq y \leq 0. \quad (3d)$$

Continuity condition

$$T_1(x, 0) = T_2(x, 0), \quad |x| \leq a, \quad (4)$$

where T_f denotes the environment temperature and h is the convective heat-transfer coefficient.

2.3. Solution to Eqs. (1) and (2)

The solution of Eqs. (1) and (2) can easily be found by taking into account Eqs. (3d) and (4). They are written as

$$T_1(x, y) = \frac{q}{k_1} y + C_0 + \sum_{n=1}^{\infty} (C_n + D_n) \cos \frac{n\pi x}{b}, \quad (5)$$

$$T_2(x, y) = C_0 + D_0 y + \sum_{n=1}^{\infty} (C_n e^{-\omega_n y} + D_n e^{\omega_n y}) \cos \frac{n\pi x}{b}, \quad (6)$$

where constants C_0, D_0, C_n and D_n ($n = 1, 2, 3 \dots$) can be determined by Eqs. (3a)–(3c). They are expressed as

$$\begin{aligned} C_0 &= T_f + \left(t_2 + \frac{k_2}{h} \right) \frac{qa}{k_2 b}, \quad D_0 = \frac{qa}{k_2 b}, \\ C_n &= \frac{a_n r_n e^{-2\omega_n t_2}}{\omega_n (1 - r_n e^{-2\omega_n t_2})}, \quad D_n = \frac{a_n}{\omega_n (1 - r_n e^{-2\omega_n t_2})}, \\ a_n &= \frac{2q}{n\pi k_2} \sin \frac{n\pi a}{b}, \quad r_n = \frac{\omega_n - h/k_2}{\omega_n + h/k_2}, \\ \omega_n &= n\pi/b. \end{aligned} \quad (7)$$

From Eqs. (5) and (6), it can be found that the temperature fields $T_1(x, y)$ and $T_2(x, y)$ satisfy Eqs. (3d) and (4).

3. Thermal stress field

As shown in Fig. 3, Young's modulus, Poisson's ratio and thermal expansion coefficient of the chip are denoted by the symbols E_1, μ_1 and α_1 , respectively, while E_2, μ_2 and α_2 represent the corresponding material parameters of the substrate. It should be shown that the chip and the substrate in Fig. 3 have the same

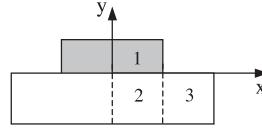


Fig. 3. The thermo-mechanical model of chip-substrate structure.

geometrical parameters with ones in Fig. 1 and only the thermal load $\Delta T(x, y)$ with symmetry on the y -axis is considered.

For the problem of thermoelasticity, the corresponding basic equations in the absence of body force can be written in the following form:

Divergence equation

$$\sigma_{ij,j} = 0, \quad (8)$$

where σ_{ij} is the stress tensor.

Constitutive equation

$$\varepsilon_{ij} = B_{ijkl}\sigma_{kl} + (1 + \nu)\alpha T \delta_{ij}, \quad (9)$$

where ε_{ij} is the strain tensor, T is the temperature field in the structure, δ_{ij} is the Kronecker delta and B_{ijkl} , ν and α is the elastic compliance, Poisson's ratio and thermal expansion coefficient of materials, respectively.

Gradient equation

$$\varepsilon_{ij} = (u_{i,j} + u_{j,i})/2, \quad (10)$$

where u_i is the elastic displacement.

When the thermal load $\Delta T(x, y)$ is applied, the elastic field in the structure should satisfy the equilibrium equation $\delta\sigma_{ij,j} = 0$ in terms of the variational principle. Thus, according to the Gauss divergence theorem, we have

$$\int \int_s u_i \delta\sigma_{ij,j} dx dy = \int_{\Gamma} u_i \delta\sigma_{ij} n_j dl - \int \int_s u_{i,j} \delta\sigma_{ij} dx dy = 0, \quad (11)$$

where s and Γ denote the area and the boundary of the chip-substrate structure, respectively, and $\delta\sigma_{ij}$ represents the variation for the stress component σ_{ij} . Considering the traction-free conditions on the boundary and utilizing Eq. (11), we have

$$\int \int_s u_{i,j} \delta\sigma_{ij} dx dy = 0. \quad (12)$$

Following the symmetry of the present problem, only half of the chip-substrate structure needs to be considered. As shown in Fig. 3, taking the right half and dividing it into three rectangular regions, the displacement and stress fields corresponding to three different rectangular regions s_k are denoted by $u_i^{(k)}$ and $\sigma_{ij}^{(k)}$ ($k = 1, 2, 3$), respectively. Hence, Eq. (12) may be written as

$$\sum_{k=1}^3 \int \int_{s_k} u_{i,j}^{(k)} \delta\sigma_{ij}^{(k)} dx dy = 0. \quad (13)$$

Substituting Eqs. (10) and (9) into Eq. (13) yields

$$\sum_{m=1}^3 \int \int_{s_m} \left(B_{ijkl}^{(m)} \sigma_{kl}^{(m)} \delta\sigma_{ij}^{(m)} + (1 + \nu_m) \alpha_m T_m \delta\sigma_{ii}^{(m)} \right) dx dy = 0, \quad (14)$$

where $B_{ijkl}^{(m)}$, v_m , α_m and T_m denote the elastic compliance, Poisson's ratio, thermal expansion coefficient and temperature field in the m th region, respectively. For the stress field, the corresponding boundary conditions and continuity conditions on the interface are as follows:

Boundary conditions

$$\begin{cases} \sigma_{11}^{(1)}(a, y) = \sigma_{12}^{(1)}(a, y) = 0, & 0 \leq x \leq a, \quad 0 \leq y \leq t_1, \\ \sigma_{22}^{(1)}(x, t_1) = \sigma_{12}^{(1)}(x, t_1) = 0, \end{cases} \quad (15a)$$

$$\begin{cases} \sigma_{11}^{(3)}(b, y) = \sigma_{12}^{(3)}(b, y) = 0, \\ \sigma_{22}^{(3)}(x, 0) = \sigma_{12}^{(3)}(x, 0) = 0, \\ \sigma_{22}^{(3)}(x, -t_2) = \sigma_{12}^{(3)}(x, -t_2) = 0, \end{cases} \quad (15b)$$

$$\sigma_{22}^{(2)}(x, -t_2) = \sigma_{12}^{(2)}(x, -t_2) = 0, \quad 0 \leq x \leq a. \quad (15c)$$

Continuity conditions

$$\begin{cases} \sigma_{22}^{(1)}(x, 0) = \sigma_{22}^{(2)}(x, 0), & 0 \leq x \leq a, \\ \sigma_{12}^{(1)}(x, 0) = \sigma_{12}^{(2)}(x, 0), \end{cases} \quad (16a)$$

$$\begin{cases} \sigma_{11}^{(3)}(a, y) = \sigma_{11}^{(2)}(a, y), \\ \sigma_{12}^{(3)}(a, y) = \sigma_{12}^{(2)}(a, y), \end{cases} \quad -t_2 \leq y \leq 0, \quad (16b)$$

where Eq. (16a) indicates the continuity of peeling (normal) and shear stresses across the interface between regions 1 and 2 and Eq. (16b) shows the continuity of normal and shear stresses across the interface between regions 2 and 3. In addition to the conditions mentioned above, the symmetric condition on the y -axis can be written as

$$\sigma_{12}^{(1)}(0, y) = \sigma_{12}^{(2)}(0, y) = 0, \quad -t_2 \leq y \leq t_1. \quad (17)$$

The stress field in the chip-substrate structure is completely determined by Eq. (14) and conditions (15)–(17). To solve the present problem, we introduce the stress functions $\Phi^{(k)}(x, y)$ ($k = 1, 2, 3$). Thus, the stress field corresponding to different regions may be expressed in terms of $\Phi^{(k)}(x, y)$ as

$$\begin{aligned} \sigma_{xx}^{(k)}(x, y) &= \Phi_{yy}^{(k)}(x, y), \\ \sigma_{yy}^{(k)}(x, y) &= \Phi_{xx}^{(k)}(x, y), \\ \tau_{xy}^{(k)}(x, y) &= -\Phi_{xy}^{(k)}(x, y). \end{aligned} \quad (18)$$

To construct the stress functions, we first define the nondimensional coordinate η along the thickness. It can be expressed as

$$\eta = \frac{y - y_b^{(i)}}{y_t^{(i)} - y_b^{(i)}} \quad (i = 1, 2, 3), \quad (19)$$

where $y_b^{(i)}$ and $y_t^{(i)}$ are, respectively, the coordinates of the bottom surface and the top surface in the i th region. Thus, the coordinate η in each region varies from 0 to 1. Since the thicknesses of the chip and the substrate are smaller in comparison with the sizes of other two directions, the in-plane stresses can approximately be taken as the polynomial distribution along the thickness direction. Hence, the stress function in each region may be approximated by a polynomial function in the normalized coordinate η . In the present analysis, the stress functions are expanded into polynomials of degree five. These stress func-

tions that satisfy the second equation of Eq. (15a), the second and third equations of Eqs. (15b)–(16a) are given by

$$\begin{aligned}\Phi^{(1)}(x, \eta) &= (1 - 3\eta^2 + 2\eta^3)F(x) + (\eta - 2\eta^2 + \eta^3)t_1G(x) + \eta^2(1 - \eta)^2P_1(x) + \eta^2(1 - \eta)^3Q_1(x), \\ \Phi^{(2)}(x, \eta) &= (3\eta^2 - 2\eta^3)F(x) + (\eta^3 - \eta^2)t_2G(x) + \eta^2(1 - \eta)^2P_2(x) + \eta^3(1 - \eta)^2Q_2(x), \\ \Phi^{(3)}(x, \eta) &= \eta^2(1 - \eta)^2P_3(x) + \eta^3(1 - \eta)^2Q_3(x).\end{aligned}\quad (20)$$

The first equation of Eq. (15a), the first equation of Eqs. (15b), (16b) and (17) can be satisfied by taking into account the following relations:

$$\begin{cases} F(a) = G(a) = P_1(a) = Q_1(a) = 0, \\ F'(a) = G'(a) = P'_1(a) = Q'_1(a) = 0, \end{cases}\quad (21a)$$

$$P_3(b) = Q_3(b) = P'_3(b) = Q'_3(b) = 0, \quad (21b)$$

$$\begin{cases} P_2(a) = P_3(a), Q_2(a) = Q_3(a), \\ P'_2(a) = P'_3(a), Q'_2(a) = Q'_3(a), \end{cases}\quad (21c)$$

$$F'(0) = G'(0) = P'_1(0) = Q'_1(0) = P'_2(0) = Q'_2(0) = 0 \quad (21d)$$

where the prime denotes the derivative with respect to variable x , for example,

$$f'(c) = df(x)/dx|_{x=c}.$$

Substituting Eq. (20) into Eqs. (18) and (14), performing the integral with respect to variable η and integrating by parts with respect to x , we obtain

$$W \frac{d^4X}{dx^4} + V \frac{d^2X}{dx^2} + UX = R, \quad (22)$$

where U , V and W are real symmetric matrices of the order 8×8 , R is an 8×1 vector (see Appendix A) and $X(x) = [F(x), G(x), P_1(x), Q_1(x), P_2(x), Q_2(x), P_3(x), Q_3(x)]^T$ is an unknown 8×1 vector. From Eqs. (21) and (22), it can be seen that the present problem is changed into the one-dimensional eigenvalue problem. According to the theory of differential equation, Eq. (22) can easily be solved. After the solution $X(x)$ is determined, the stress field may be determined by substituting $X(x)$ into Eqs. (20) and (18). The peeling and shear stresses on the interface between the chip and the substrate are given by

$$\sigma = F''(x), \quad \tau = -G'(x), \quad (23)$$

where $\sigma = \sigma_{22}(x, 0)$ and $\tau = \sigma_{12}(x, 0)$.

4. Results and discussions

Parameters in Table 1 are chosen to simulate practical packaging structures. In addition, the heat flux density, environment temperature and convective heat-transfer coefficient are taken as $q = 0.1 \text{ W/mm}^2$, $T_f = 60^\circ\text{C}$ and $h = 0.012 \text{ W/mm}^2\text{K}$, respectively. Applying the temperature field in the form of difference between the temperature field solved in Section 2.1 and the room temperature 25°C , the method introduced in this paper is used to calculate the interfacial peeling and shear stresses between the chip and the substrate.

To compare the present results with the numerical ones, the ANSYS program is used to make a finite element analysis in this paper. In the finite element analysis, the triangular element is adopted and refined

Table 1
Physical parameters

Structures	Materials	Width (mm)	Thickness (mm)	Thermal conductivity (W/mm K)	CTE $\times 10^{-6}^{\circ}\text{C}$	Young's modulus (GPa)	Poisson's ratio
Chip	Si	7.01	0.381	0.1716	2.5	200	0.3
Substrate	Al_2O_3	11.63	0.889	0.025	6.8	283	0.2

meshes are used near the free edge. Fig. 4 shows the variations of interfacial thermal stresses along the x -axis. In Fig. 4, the capital letters PM and FEM represent the results given by the present method and the finite element one, respectively. From this figure, it can be seen that the interfacial stresses tend towards zero with the increasing of the distance from the free edge. This agrees with numerical results obtained by FEM. However, there are larger differences between the present results and ones of FEM near the free edge. The shear stress given by FEM has a maximum at the edge. This violates the fact that the shear stress equals zero at the free edge. However, the shear stress obtained by the present method satisfies the requirement mentioned above. In addition, it can also be found that the interfacial peeling stress is positive and finite compared to the interfacial shear stress. Therefore, the interfacial peeling stress should be considered while analyzing the delamination failure of the interface between the chip and the substrate. Thus, some previous works that only consider the effect of the interfacial shear stress on delamination failure should be revised.

Figs. 5 and 6 represent the distributions of interfacial peeling stress and shear stress along the x -axis when the substrate/chip thickness ratio t_2/t_1 is taken as 1, 2, 5, and 10, respectively. From these two figures, we find that the substrate/chip thickness ratio has a prominent effect on the distributions of interfacial thermal stresses between the chip and the substrate. The position of maximums for the stress field approaches to the free edge and the variation of the stress field is steeper when t_2/t_1 becomes small.

Since the increasing of the chip area is a tendency in the development of microelectronic packaging, the variation of interfacial thermal stresses with the chip area is very important for guiding the design of packaging structures. As shown in Figs. 7 and 8, six sets of data corresponding to $a/b = 0.1, 0.3, \dots, 1.0$ are calculated when only the chip area varies. Numerical results show that the positions of maximums of stress components depart gradually from the free edge with the decreasing of the chip area. Although the peak value of the stress field does not vary with the chip area, the stress concentration becomes weak when a/b decreases.

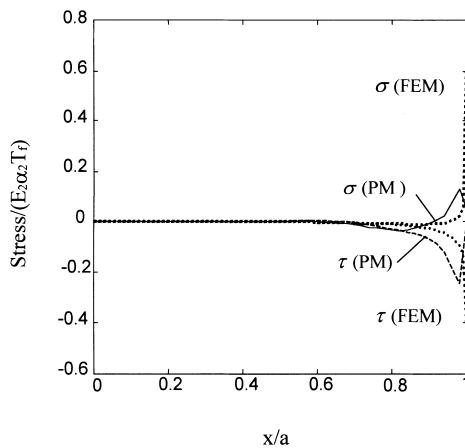
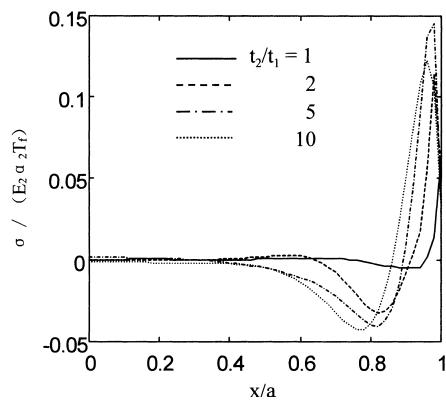
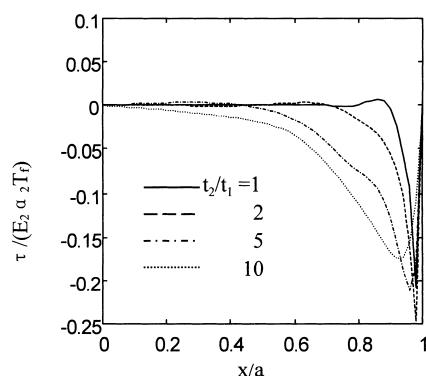
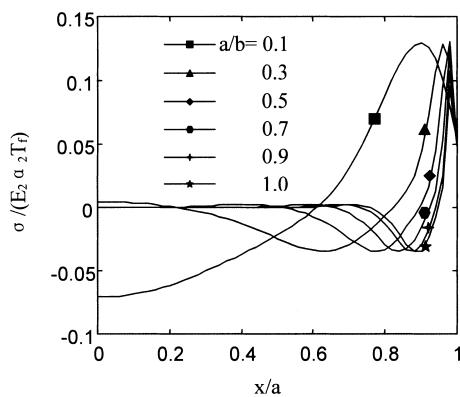


Fig. 4. Comparison of interfacial thermal stresses between analytical solution and FEM.

Fig. 5. Distribution of interfacial peeling stress along the x -axis.Fig. 6. Distribution of interfacial shear stress along the x -axis.Fig. 7. Variation of interfacial peeling stress along the x -axis for different chip areas.

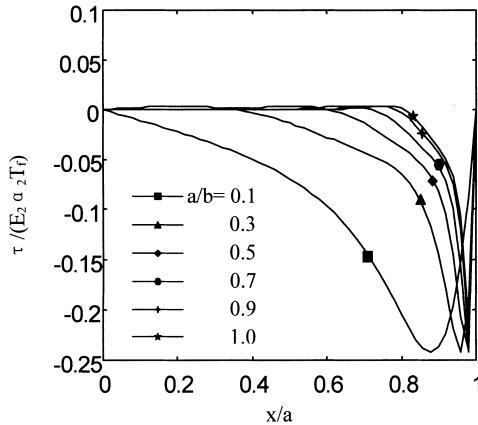


Fig. 8. Variation of interfacial shear stress along the x -axis for different chip areas.

5. Conclusions

A simple model by taking into account the heat conduction mechanism of the system is established. The corresponding temperature field is solved. According to the temperature field obtained, the stress field induced by the symmetric thermal load is determined by the variational principle. The distribution of the interfacial thermal stresses and the edge effect are analyzed in details. From the numerical results, it can be found that (1) the interfacial peeling stress should be considered in investigating the delamination failure between the chip and the substrate. (2) The substrate/chip thickness ratio has an important effect on the distribution of the interfacial thermal stresses. (3) The chip area has some effect on the distribution of the interfacial thermal stresses.

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Appendix A

Here, the determination of matrices U , V and W and vector R is discussed in detail. Eq. (20) can be written as

$$\Phi^{(i)}(x, \eta) = A_i(\eta)X(x) \quad (i = 1, 2, 3), \quad (\text{A.1})$$

where $A_i(\eta)$ are 1×8 matrices and can be expressed as

$$\begin{aligned} A_1 &= \left[1 - 3\eta^2 + 2\eta^3, t_1(\eta - 2\eta^2 + \eta^3), \eta^2(1 - \eta)^2, \eta^2(1 - \eta)^3, 0, 0, 0, 0 \right], \\ A_2 &= \left[3\eta^2 - 2\eta^3, t_2(\eta^3 - \eta^2), 0, 0, \eta^2(1 - \eta)^2, \eta^2(1 - \eta)^3, 0, 0 \right], \\ A_3 &= \left[0, 0, 0, 0, 0, 0, \eta^2(1 - \eta)^2, \eta^2(1 - \eta)^3 \right]. \end{aligned} \quad (\text{A.2})$$

Substituting Eq. (A.1) into Eq. (18), the stress field in different regions can be written as

$$\sigma_{11}^{(i)} = D_i X, \quad \sigma_{22}^{(i)} = A_i X'', \quad \sigma_{12}^{(i)} = B_i X' \quad (i = 1, 2, 3), \quad (\text{A.3})$$

where X' and X'' are, respectively, the first and second derivatives of vector X with respect to variable x and B_i and D_i , respectively, the first and second derivatives of vector A_i with respect to variable η , namely,

$$B_1 = -\frac{1}{t_1} \frac{dA_1}{d\eta}, \quad B_2 = -\frac{1}{t_2} \frac{dA_2}{d\eta}, \quad B_3 = -\frac{1}{t_2} \frac{dA_3}{d\eta}, \quad (\text{A.4})$$

$$D_1 = \frac{1}{t_1^2} \frac{d^2 A_1}{d\eta^2}, \quad D_2 = \frac{1}{t_2^2} \frac{d^2 A_2}{d\eta^2}, \quad D_3 = \frac{1}{t_2^2} \frac{d^2 A_3}{d\eta^2}. \quad (\text{A.5})$$

Performing the variation for the stress field in (A.3), we can obtain

$$\delta\sigma_{11}^{(i)} = D_i \delta X, \quad \delta\sigma_{22}^{(i)} = A_i \delta X'', \quad \delta\sigma_{12}^{(i)} = B_i \delta X' \quad (i = 1, 2, 3), \quad (\text{A.6})$$

where δX , $\delta X'$ and $\delta X''$ denote the variations of vectors X , X' and X'' , respectively. Substituting Eqs. (A.6) and (A.3) into Eq. (14) and integrating by parts with respect to variable x , we can obtain by taking into account Eq. (19) and performing some manipulation

$$\int_0^b \left(W \frac{d^4 X}{dx^4} + V \frac{d^2 X}{dx^2} + UX - R \right) \delta X \, dx = 0. \quad (\text{A.7})$$

It should be noted that the different components of vector X in Eq. (A.7) have different variable ranges, for example, the variable of functions $F(x)$, $G(x)$, $P_1(x)$, $Q_1(x)$, $P_2(x)$ and $Q_2(x)$ varies in the range $[0, a]$ and $P_3(x)$ and $Q_3(x)$ have the variable range $[a, b]$. Since δX is arbitrary, Eq. (A.7) may be written as

$$W \frac{d^4 X}{dx^4} + V \frac{d^2 X}{dx^2} + UX = R, \quad (\text{A.8})$$

where U , V and W are real constant matrices of order 8×8 and R is an 8×1 vector, which can be expressed as

$$\begin{aligned} U &= \int_0^1 \left[\frac{t_1(1-v_1^2)}{E_1} D_1^T D_1 + \frac{t_2(1-v_2^2)}{E_2} (D_2^T D_2 + D_3^T D_3) \right] d\eta, \\ V &= - \int_0^1 \left[\frac{t_1 v_1 (1+v_1)}{E_1} (D_1^T A_1 + A_1^T D_1) + \frac{t_2 v_2 (1+v_2)}{E_2} (D_2^T A_2 + A_2^T D_2 + D_3^T A_3 + A_3^T D_3) \right. \\ &\quad \left. + \frac{2t_1(1+v_1)}{E_1} B_1^T B_1 + \frac{2t_2(1+v_2)}{E_2} (B_2^T B_2 + B_3^T B_3) \right] d\eta, \\ W &= \int_0^1 \left[\frac{t_1(1-v_1^2)}{E_1} A_1^T A_1 + \frac{t_2(1-v_2^2)}{E_2} (A_2^T A_2 + A_3^T A_3) \right] d\eta, \\ R &= \int_0^1 \left\{ t_1(1+v_1) \alpha_1 \left(\Delta T_1 D_1^T + \frac{\partial^2 \Delta T_1}{\partial x^2} A_1^T \right) \right. \\ &\quad \left. + t_2(1+v_2) \alpha_2 \left[\Delta T_2 (D_2^T + D_3^T) + \frac{\partial^2 \Delta T_2}{\partial x^2} (A_2^T + A_3^T) \right] \right\} d\eta. \end{aligned} \quad (\text{A.9})$$

It should be shown that the following relations are used in the derivation of Eq. (A.9)

$$\begin{aligned} B_{1111}^{(1)} &= B_{2222}^{(1)} = \frac{1-v_1^2}{E_1}, & B_{1122}^{(1)} &= B_{2211}^{(1)} = \frac{v_1(1+v_1)}{E_1}, & B_{1212}^{(1)} &= \frac{2(1+v_1)}{E_1}, \\ B_{1111}^{(m)} &= B_{2222}^{(m)} = \frac{1-v_2^2}{E_2}, & B_{1122}^{(m)} &= B_{2211}^{(m)} = \frac{v_2(1+v_2)}{E_2}, & B_{1212}^{(m)} &= \frac{2(1+v_2)}{E_2}, \quad (m = 2, 3), \end{aligned} \quad (\text{A.10})$$

where ν and E are Poisson's ratio and Young's Modulus of materials. Thus, the matrices U , V and W and vector R are fully determined by Eq. (A.9).

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